UNIT V - BLOCKING OSCILLATORS AND TIME BASE GENERATORS


5.0 INTRODUCTION:

A pulse transformer may be used to couple the output of an active device back to the input.

If the relative winding polarities are properly chosen, the feedback will be regenerative and the circuit can be made to generate a single pulse (monostable) or a train of pulses (astable).

A transformer coupled configuration which is of considerable practical importance, is a blocking oscillator.

Astable and monostable blocking oscillators are discussed here.

5.1 Monostable Blocking Oscillator Using Emitter Based Timing:

CONSTRUCTION:

A monostable blocking oscillator is shown in the figure.

It consists of a transistor with an emitter resistor and a 3 winding pulse transformer.

One winding is present in the collector circuit, the second winding with n times turns in the base circuit, the third winding with n1 times as many turns as the collector winding feeds the resistor R1 which may be the load or may be required for damping.

The base and the collector turns must be connected for regenerative but the relative winding direction for the third leg of the transformer may be arbitrary.

It may be chosen to obtain either a positive or negative output pulse across the load.
OPERATION:
➢ The equivalent circuit from which the current and voltage waveforms are calculated is shown.

Fig(a): A monostable blocking oscillator with emitter timing

Fig(b): The equivalent circuit during pulse formation

Applying KVL to the outside loop encompassing both the collector gives
The collector current waveform is trapezoidal with a positive slope, the base current is also trapezoidal but with a negative slope and the emitter current is constant during the pulse.

At \( t=0^+ \), \( i_c < hfe \cdot i_b \) and the transistor is in saturation.

Or the drop \( V \) across the collector winding during the pulse is

\[
V = \frac{V_{cc}}{(n+1)}
\]

From the base circuit it is seen that the drop across \( R \) is

\[
V_{en} = nV = (i_c - i_b)R
\]

Or

\[
-i_e = i_c' + i_b = nV/R = \frac{n}{n+1}(V_{cc}/R)
\]

Note that the emitter current is constant. In order to find the collector and base currents individually, one more relation between \( i_c \) and \( i_b \) should be noted. Since the sum of the ampere turns in the ideal transformer is zero,

\[
I + n i_b + n i_l = 0
\]

From the load circuit,

\[
i_l = -\left(\frac{n V}{R_L}\right)
\]

From KCL at the collector node

\[
i = i_c + i_m = i_c - \frac{V_{cc}}{L}
\]

Substituting from eq 6 and 7 in 5

\[
i_c = \frac{V_{cc}}{L} - n i_b - \left(\frac{n^2 V}{R_L}\right) = 0
\]

This is the desired second relationship between \( i_c \) and \( i_b \). solving eq 4 and 8 using \( i_c \) we get

\[
i_c = \frac{V_{cc}}{(n+1)^2} \left( \frac{n^2}{R} + \frac{n_1^2}{R_L} + \frac{t}{L} \right)
\]

\[
i_b = \frac{V_{cc}}{(n+1)^2} \left( \frac{n}{R} - \frac{n_1^2}{R_L} + \frac{t}{L} \right)
\]
- As the time passes, $ic$ increases and the operating point moves up the saturation line.
- While $ic$ grows with time, the base current is decreasing and reaches a point where $i=I_b$ and $ic=hfe.I_b$.
- Applying this to equations 9 and 10, we get

$$tp = \frac{nL}{R} \frac{hfe - n}{hfe + 1} - \frac{n^2 L}{R_L}$$

since usually $1/5 < n < 1$, then $hfe >> n$ and

$$tp \approx (nL/R) - (n^2 L/R_L)$$

- Subject to the approximations made above, the pulse width $tp$ is independent of $hfe$ and depends only upon passive elements $n$, $I_b$, $R$, etc.
- Here, then it yields a pulse of very stable duration.
- If the second term in equation 12 exceeds the first term, then $tp$ is negative, which situation is obviously impossible.
- In order for the loop gain to exceed unity, which is the necessary condition for regeneration to take place and pulse to form, the following inequality must be valid.

$$R_L = \frac{n^2 R (hfe + 1)}{n (hfe - n)}$$

Fig: The current and voltage waveforms in a transistor-blocking oscillator.
If this inequality is satisfied then $t_p$ in eq 11 cannot be negative.

The effect of the transistor saturation voltages on the pulse width is to multiply the first term in eq 11 by the factor

$$F = \frac{V_{cc} - V_{ce\ (sat)} - [V_{be\ (sat)}/n]}{V_{cc} - V_{ce\ (sat)} + V_{be\ (sat)}}$$

Hence as long as $V_{cc} > V_{ce\ (sat)} + [V_{be\ (sat)}/n]$ then the pulse duration is almost independent of supply voltage and is given by eq 13.

Here the effect of base spreading resistance is neglected.

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**Fig:** The load $R_i$ is switched on and off through $Q_2$

The waveforms for $t > t_p$ is now examined.

At the termination of the pulse there exists a current $i_m$ in the magnetizing inductance of the transformer.

Since the current through an inductor cannot change instantaneously, the current must continue to flow even after $t = t_p$, when the transistor currents have fallen to zero.

The path for magnetizing current $i_m$ through the capacitance of the $t$. Since this capacitance is small then $i_m$ decays rapidly and induces large voltage overshoots at the collector, base, and at the load as indicated in the figure.

These overshoots must not be so large so as to exceed the breakdown voltage $Bv_{ce}$ or $Bv_{be}$.

It is important to note that adequate damping of the backswing which occurs at the termination of the pulse is absolutely essential to the operation of the blocking oscillator.

In the figure (e) the solid curve represents the typical waveform when damping is sufficient to cause the backswing to die down in a half cycle.

If the damping is inadequate the backswing may oscillate as indicated by the dashed curve.

In such a case regeneration would start again at the point marked $X$, where the base voltage is slightly positive and the transistor reenters the active region.

The blocking oscillator would then be free running and would generate a continuous oscillation whose shape would resemble a very distorted sinusoid.
If the core losses of the transformer are low, as they are in a ferrite core and if the load RL does not supply adequate damping then an external resistor must be shunted across the transformer in order to obtain monostable operation.

In order to suppress the transformer oscillations without loading the blocking oscillator during the pulse interval, damping resistor R’ in series with a diode may be shunted across the transformer.

The diode is introduced with such polarity that it does not conduct during the pulse interval but does during the overshoot.

With an n — p — n transistor the anode of the diode is at the collector side and the cathode at the supply voltage side.

The resistor R’ is selected to be smaller that the critical damping resistance. At the end of the pulse the diode conducts and the energy stored in the magnetizing inductance is dissipated in R’ with a time constant 1/k’.

Allowing four time constants for the quiescent condition to be established, the maximum frequency at which the circuit can be triggered is fmax = R’/4L

The load to be driven by the blocking oscillator may be supplied from a tertiary winding or placed across R from emitter to ground.

In either case from equation 13 we see that the pulse width depends upon the value of the load resistance.

There are applications where the blocking oscillator must drive, variable load for example a ferrite core, memory where the load depends on the number of cores to be excited.

A method of obtaining a pulse duration which is independent of loading is to place RL in the collector leg of the second transistor Q2 whose base current is the collector current of blocking oscillator transistor Q1 as shown in figure.

The effective supply voltage of Q1 is Vcc-Vbe2(sat)≈Vcc.

The load current is (Vcc-Vce2(sat))/RL=Vcc/RL for a time tp=nI/R and zero outside the interval.

**Control of pulse duration using core saturation:**

In the common emitter circuit the transformer coupling is between the collector and the base.

It is also possible place one winding of the transformer in the collector and the second winding in the emitter resulting in a common base configuration.

A third possibility employs transformer coupling between the base and the, emitter, a common collector configuration.

In each case it is found that if the timing resistor R is in the base, tp varies drastically with hfe, whereas if R in the emitter tp is almost independent of hfe.

So the timing resistor should be placed in the emitter, but there is no distinct advantage in one coupling method over the others.

However the CE configuration generates output pulses of opposite polarity at the two windings, whereas the CB and CC do not.

In deriving equation 13 for tp it is implicitly assume that the magnetizing inductance L is a constant.

Consider a core that saturates When the flux density B reaches the maximum value Bm.

The inductance L now decreases with current and L→0 as B→Bm.
From eq 9 and 10 we may anticipate that the collector and the base currents will no longer be trapezoidal but rather will have wave shape more like those indicated in the figure.

As $B \rightarrow B_m$, $i_c$ increases very rapidly whereas $i_b$ decreases to zero.

Hence as the maximum flux density is approached the condition $i_c = hfe \cdot i_b$ is satisfied and the pulse ends.

Assume that the pulse ends when the core is completely saturated.

Let $N$ equal the number of turns in the collector winding, $A$ equal the cross sectional area of the core $\phi$ the magnetic flux.

The voltage hence across the collector winding is a constant $V$ and

$$V = N \phi / dt = NA \cdot dB / dt = Vcc / (n+1)$$

Integrating between the limits 0 and $t_p$ for $t$, corresponding to 0 and for $B$ given,

$$t_p = \frac{(n + 1)NABm}{Vcc}$$

It should be noted that the pulse duration depends upon the supply voltage and the properties of the core but not upon the transistor parameters.

Now consider a core which in addition to saturation also exhibits hysteresis as indicated in the $B-H$ loop.

Assume that at $t = 0$, with no current in the windings, $B = -Br$, and when the blocking oscillator is triggered, $H$ increases beyond $Hc$, so that $B$ reaches $Br$.

Then $t_p$ is given by equation 14 With $B_m$ replaced by $2Br$.

At the end of the pulse $B$ retains the residual flux density $Br$.

An attempt to trigger the blocking oscillator again is now doomed to failure because $dB/dt = 0$, no voltages are induced in the transformer, and regeneration is impossible.

In order for, the circuit to operate properly the core must be reset so that its flux is $-Br$ after each pulse.

A convenient method of obtaining this reset flux is to use an auxiliary winding in series with a resistor $R_r$ across the supply voltage.

When the transistor is off the current $Vcc/R_r$ in this reset winding supplies the necessary ampere turns so that $H$ becomes more negative than $-Hc$ and hence $B = -Br$. 

Fig: A rectangular hysteresis loop for an iron core
Fig A shorted delay line used to determine the pulse width of the blocking Oscillator.

- The figure shows a shorted delay line for controlling pulse the pulse width.
- When the blocking oscillator is triggered, a positive-step is generated at the input to the line.
- This discontinuity upon reaching the shorted end of the line at \( t=td \), is reversed in polarity.
- When this reflected wave reaches the input to the line, the positive step at the collector to the transistor starts the regenerative action which terminates the blocking oscillator pulse.
- The width of the pulse is \( 2td \), provide that \( tp \) as determined by eq 13 is greater that \( 2td \).

5.2 ASTABLE BLOCKING OSCILLATOR;

- When power is applied to the circuit, R1 provides forward bias and transistor Q1 conducts.
- Current flow through Q1 and the primary of Te induces a voltage in L2.
- The phasing dots on the transformer indicate 180-degree phase shift.
- As the bottom side of L1 is going negative, the bottom side of L2 is going positive.
- The positive voltage of L2 is coupled to the base of the transistor through C1, and Q1 conducts more.
- This provides more collectors current and more current through L1.
- This action is regenerative feedback.
- Very rapidly, sufficient voltage is applied to saturate the base of Q1.
- Once the base becomes saturated, it loses control over collector current.
- The circuit now can be compared to a small in series with a relatively C large inductor (L1), or a series RL circuit.
- The operation of the circuit to this point has generated a very steep leading edge for the output pulse.
- Figure shows the idealized collector and base waveforms.
- Once the base of Q1 becomes saturated, the current increase in L1 is determined by the time constant of L1 and the total series resistance.
- From T0 to T1 in figure the current increase (not shown) is approximately linear.
- The voltage across L1 will be a constant value as long as the current increase through L1 is linear.

Fig: Blocking oscillator.

Fig: Blocking oscillator idealized waveforms.
At time T1, L1 saturates.

At this time, there is no further change in magnetic flux and no coupling from L1 to L2.

C1, which has charged during time to T0 to T1, will now discharge through R1 and cut off Q1.

This causes collector current to stop, and the voltage across LI returns to 0.

The length of time between T0 and T1 (and T2 to T3 in the next cycle) is the pulse width, which depends mainly on the characteristics of the transformer and the point at which the transformer saturates.

A transformer is chosen that will saturate at about 10 percent of the total circuit current.

This ensures that the current increase is nearly linear.

The transformer controls the pulse width because it controls the slope of collector current increase between points T0 and T1.

Since TC = L / R, the greater the L, the longer the TC.

The longer the time constant, the slower the rate of current increase.

When the rate of current increase is slow, the voltage across L1 is constant for a longer time.

This primarily determines the pulse width.

From T1 to T2, transistor Q1 is held at cutoff by C1 discharging through R1.

The transistor is now said to be “blocked.”

As C1 gradually loses its charge, the voltage on the base of Q1 returns to a forward-bias condition.

At T2, the voltage on the base has become sufficiently positive to forward bias Q1, and the cycle is repeated.

The collector waveform may have an inductive overshoot (parasitic oscillations) at the end of the pulse.

When Q1 cuts off, currents through L1 ceases, and the magnetic field collapses, inducing a positive voltage at the collector of Q1.

These oscillations are not desirable, so some means must be employed to reduce them.

The transformer primary may be designed to have a high dc resistance resulting in a low Q, this resistance will decrease the amplitude of the oscillations.
However, more damping may be necessary than such a low-Q transformer primary alone can achieve. If so, a DAMPING resistor can be placed in parallel with L1, as shown in figure.

When an external resistance is placed across a tank, the formula for the Q of the tank circuit is $Q = R/XL$, where R is the equivalent total circuit resistance in parallel with L.

You should be able to see from the equation that the Q is directly proportional to the damping resistance (R).

In figure damping resistor R2 is used to adjust the Q which reduce the amplitude of overshoot parasitic oscillations.

As R2 is varied from infinity toward zero, the decreasing resistance will load the transformer to the joint that pulse amplitude, width, and prf are affected.

If reduced enough, the oscillator will cease to function.

By varying R2, varying degrees of damping can be achieved, three of which are shown in figure (A), (B) and (C).
CRITICAL DAMPING gives the most rapid transient response without overshoot.

- This is accomplished by adjusting R2 to achieve a waveform as shown in fig (A).
- The resistance of R2 depends upon the Q of the transformer.
- View (A) shows that oscillations, including the overshoot, are damping out.

- UNDERDAMPING gives rapid transient response with overshoot caused by high or infinite resistance as shown in figure (B).

- OVERDAMPING is caused by very low resistance and gives a slow transient response.

- It may reduce the pulse amplitude as shown in fig (C).
PULSE TRANSFORMER:

- The blocking oscillator discussed is a free-running circuit.
- For a fixed prf, some means of stabilizing the frequency is needed.
- One method is to external synchronization triggers.
- Coupling capacitor C2 feeds input synchronization triggers to the base of Q1.

![Fig(A). Blocking oscillator (synchronized).]

- If the trigger frequency is made slightly higher than the free-running frequency, the blocking oscillator will 'lock in' at the higher frequency.
- For instance; assume the free-running frequency of this blocking oscillator is 2 kilohertz, with a part of 500 microseconds.
- If sync pulses with a prt of 400 microseconds, or 2.5 kilohertz, are applied to the base, the blocking oscillator will “lock in” and run at 2.5 kilohertz.
- If the sync prf is too high, however, frequency division will occur.
- This means that if the sync prt is too short, some of the triggers occur when the base is far below cutoff.
- The blocking oscillator may then synchronize every second or third sync pulse.
- For example, in fig (A) and view(B) if trigger pulses are applied every 200 microseconds (5 kilohertz), the trigger that appears at T1 is not of sufficient amplitude to overcome the cutoff bias and turn on Q1.
At T2, capacitor C1 has nearly discharged and the trigger causes Q1 to conduct.
Note that with a 200- microsecond input trigger the output prt is 400 microseconds.
The output frequency is one-half the input trigger frequency and the blocking oscillator becomes a frequency divider.

INVERTER:

A blocking astable is shown at the right.
The 10k resistor pull up has been removed so the normal state of the transistor is “off.”
A positive pulse at node “a” will start conduction, and the transformer will do the rest. After the brief excursion 0 conduction, in which the output falls to near ground, the transistor will again be turned off (by a hefty negative pulse to the base).
In this circuit, the trigger pulse are provided by an RC differentiating circuit, which produces narrow pulse alternately positive and negative.
The astable responds only to the positive pulse which need only be about 1V high.
For every positive pulse, the circuit will produce one low-going pulse of brief duration.
If the circuit is followed by a phase inverter, the pulses will be a normal string or positive pulses.
No effort has been made to make the pulses as short as possible these will be 100-200 micro second wide.

5.3 WAVEFORM.SHRAPING CIRCUIT:
The waveform shaping circuits like differentiating and integrating circuits are used in multivibrators as triggering and synchronizing pulse generators.
The leading and trailing edges of the trigger pulses are of utmost importance and the horizontal part of the pulse is not important in multivibrators applications.

5.3.1 RC WAVE SHAPING:
The triggering pulses to the multivibrators are to be reshaped using differentiating and integrating RC circuits.
DIFFERENTIATING CIRCUIT (high pass RC circuit):

- A simple differentiating circuit is shown below.
- It consists a series capacitor and a shunt resistor.
- Since the reactance of a capacitor is $X_c=1/(2\pi fC)$, $X_c$ decreases with increasing frequency ($f$).
- Therefore, at very high frequencies the capacitor acts as a short circuit and all the higher frequency components at the output with less attenuation than the lower frequency components.
- Hence this circuit is called high pass filter.
- The effect of time constant $\tau = RC$ on the output waveform for a input pulse signal is also shown below.

![Fig: High pass RC circuit](image)

- With reducing time constant, the pulse at the output becomes narrower with negligible sag.
- If the time constant is reduced sufficiently, the output will be simply a series of alternate positive and negative spikes.
- Mathematically, such a waveform is the first derivative of the input waveform, i.e.

$$V_o = RC \frac{dV_i}{dt}$$

- And hence, the circuit is called a differentiator.
- In general, the time constant of differentiating circuit shall be small compared to the period of the input signal.

INTEGRATING CIRCUIT (low pass RC circuit):

- The figure shows a simple, integrating circuit, consisting of a series resistor and a shunt capacitor.
- This circuit passes low frequencies of input and attenuates high frequencies because the reactance of the capacitor $C$ decreases with increasing frequency.
At very high frequencies the capacitor acts as a virtual short circuit and the output falls to zero.
Hence this circuit is called a low pass filter.
It gives an output waveform similar to the time integral of the input waveform i.e.
\[ V_o = \frac{1}{RC} \int i \, dt. \]
The output given by
\[ V_o = V_i \left[ 1 - e^{-t/RC} \right], \]
Where \( V \) is the output voltage and \( V_i \) is the input voltage.
In general, the time constant of the integrating circuit shall be large compared with the period of the input signal.

5.3.2 RL WAVE SHAPING CIRCUIT:
- We have already discussed the RC wave shaping circuit.
- The results of the RL wave shaping circuit is very similar to that of RC wave shaping circuit by replacing the capacitor \( C \) and resistor \( R \) of RC circuit by a resistor \( R' \) and an inductor \( L \) respectively and the time constants \( L/R' \) equals the time constant \( RC \).
- The inductor is seldom used if large time constant is called for because a large value of inductance can be obtained only with an iron-core inductor which is physically large, heavy and expensive relative to the cost of a capacitor for a similar application.
- Furthermore, the nonlinear properties of the iron cause distortion, which may be undesirable. If it is required to pass a very low frequency through the circuit in which \( L \) is a shunt element, then the inductor may become prohibitively large.
- The small, inexpensive, air-core inductor is used in low time constant applications.
- The below figure shows how a square wave may be converted into pulses by means of the peaking coil \( L \).
- It is assumed that the bias voltage and the magnitude of the input are such that the tube operates linearly.
When using a uni junction transistor as the switch, a simple saw tooth generator looks like the circuit in figures (A); the out wave shapes are in view(B).

When the 20 volts is applied across B2 and B 1, the n-type bar acts as a voltage-divider.
A voltage of 12.8 volts appears at a point near the emitter.
At the first instant, Cl has no voltage across it, so the of the circuit, which is taken across the capacitor (C1) is equal to 0 volts.
The voltage across Cl is also the voltage that is applied to the emitter of the uni junction.
The uni junction is now reverse biased. After TO, Cl begins to charge toward 20 volts.
At TI, the voltage across the capacitor (the voltage on the emitter) has reached approximately 12.8 volts.
This is the peak point for the uni junction, and it now becomes forward biased.
With the emitter forward biased, the impedance between the emitter and B1 is just a few ohms.
This is similar to placing a short across the capacitor.
The capacitor discharges very rapidly through the low resistance of B1 to E.
As C1 discharges, the voltage from the emitter to Base1 also decreases.
Q1 will continue to be forward biased as long as the voltage across C1 is larger than the valley point of the uni junction.

![Unijunction sawtooth generator. Emitter waveform](image)

At T2 the 3-volt valley point of the uni junction has been reached.
The emitter now becomes reverse biased and the impedance from the emitter to B1 returns to a high value.
Immediately after T2, Q1 is reverse biased then the capacitor has, a charge of approximately 3 volts.
C1 now starts to charge toward 20 volts as it did originally (just after T0).
This is shown from T0 to T3 in figure, view(B).
The circuit operation from now on is just a continuous repetition of the actions between T2 and T4.
The capacitor charges until the emitter becomes forward biased, the unijunction conducts and C1 discharges and Q1 becomes reverse biased and C1 again starts charging.
Now let's determine the linearity electrical length and amplitude of the output waveform.
First, the linearity: To charge the circuit to full 20 volts will, take 5 time constants.
In the circuit shown in, fig (B), c1 is allowed to charge from T2 to T3.
To find the percentage of charge, use the equation:
This works out to be about 57 per cent and is far beyond the 10 per cent required for a linear sweep voltage.
The linearity is very poor in this example.
The electrical length (sweep time), which is measured from T2 to T3 can be found by multiplying RC times the number of time constants.
57 percent is 0.83TC.
B multiplying 0.83 times RIC1, you will find that the electrical length is approximately 21 milliseconds:
The physical length (amplitude) is determined by subtracting the valley point from the peak point.
- This is 9.8 volts in the example (12.8 volts - 3 volts).

5.4.1 LINEARISATION:
- For a sweep generator that produces a more linear output saw tooth waveform, refer to the circuit in figure (A).
- R1 and Cl form the RC time constant.
- Notice that the capacitor charges toward 35 volts (VE) in this circuit.

The output waveform is shown in figure (B).
- With a Lower applied from B1 to B2, the peak and valley points are closer together.
- Calculating the percentage charge:

\[
\text{electrical length} = RC \times \text{number of TC} = 25 \text{k}\Omega \times 1 \mu\text{F} \times 0.33 = 20.75 \times 10^{-3} \text{ seconds} = 21 \text{ milliseconds}
\]
The linearity in this case is good.

A 10-percent charge amounts to 0.1 time constant.

The electrical length is, again, RC times the number of time constants.

With \( R_1 \) 300 kilohms and \( C_1 \) at .005 microfarads, the time constant is 1,500 microseconds.

One-tenth of a time constant is equal to 150 microseconds;
so the electrical Length is 150 microseconds.

Prt is the electrical length plus the fall or fly back time.

If \( C_1 \) discharges from 5.3 volts to 2 volts in 15 microseconds, then the prt is 150 + 15, or 165 microseconds.

The prf is about 6 kilohertz

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\[
\text{percent of charge} = \frac{E_p - E_v}{E_a - E_v} \times 100
\]

\[
= \frac{5.3 - 2}{35 - 2} \times 100
\]

\[
= \frac{3.3}{33} \times 100
\]

\[
= 10 \text{ percent}
\]

---

Some uni junction circuits are triggered to obtain a very stable prf.

One method is to apply triggers to B2, as shown in figure.

Negative triggers applied to B2 reduce the inter-base voltage enough to cause a forward bias condition in the emitter circuit.

This cuts off the sweep and allows \( C_1 \) to discharge through the B 1-to-emitter circuit.

Then, \( C_1 \) recharges until the next trigger arrives and \( C_1 \) discharges.

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Fig: Synchronized sawtooth generator.
Circuit operation and parameters are figured in the same manner as in the previous saw tooth circuits.

TRANSISTOR SAWTOOTH GENERATOR:
- The next saw tooth generator uses a conventional p n p transistor, as shown in figure (A).
- This generator also uses an RC network, and the transistor provides the switching action.

![Transistor sawtooth generator (pnp)](image)

- The waveforms for the circuit are shown in views (B) and (C).
- With no input signals, Qi is biased near saturation by R1.
- The voltage across Cl is very low (-2.5 volts) because load resistor R3 drops most of the applied voltage.
- The transistor must be cut off to allow Cl to charge.
- To cut off Qi, a positive rectangular wave is used.

![Waveforms](image)

- Since Q1 is a p n p transistor, a positive voltage must be used to drive it to cutoff.
Figure (B), shows a rectangular wave input 500 microseconds long on the positive alternation.

At T₀, the p gate applied to the base of Q₁ cuts off Q₁.

This effectively removes the transistor from the circuit (opens the switch), and C₁ charges through R₃ toward 20 volts.

Starting with a charge of -2.5 volts at T₀, C₁ charges (T₀ to T₁) for 500 microseconds to -4.25 volts at T₁.

Let’s determine the percent of charge:

\[
\text{percent of charge} = \frac{E_c^{\text{max}} - E_c^{\text{min}}}{V_{cc} - E_c^{\text{min}}} \times 100
\]

\[
= \frac{4.25 - 2.5}{20 - 2.5} \times 100
\]

\[
= \frac{1.75}{17.5} \times 100 = 10\%
\]

This allows nearly a linear rise of voltage across C₁.

Increasing the value of R₃ or C₁ increases the time constant.

The capacitor will not charge to as high a voltage in the same period of time.

Decreasing the width of the gate and maintaining the same time constant also prevents the capacitor from charging as much.

With less charge on the capacitor, and the same voltage applied, linearity has been improved.

Decreasing R₃ or C₁ or increasing gate W decreases linearity.

Changing the applied voltage will change the charge on the capacitor.

The percentage of charge remains constant; however, it does not affect linearity.

At T₁, the positive alternation of the input gate ends, and Q₁ returns to a forward-bias condition.

A transistor that is near saturation has very few resistance, so C₁ discharges rapidly between T₁ and T₂, as shown in figure (C).

The capacitor discharges in less than 200 microseconds, the length of the negative alteration of the gate.

The negative gate is made longer than the discharge time of the capacitor to ensure that the circuit has returned to its original condition.

From T₁ to T₂, the capacitor discharges and the circuit returns to its original condition, ready for another positive gate to arrive.

The next positive gate arrives at T₂ and the actions repeat.

The amplitude of the output saw tooth wave is equal to 1.75 volts (4.25 volts minus 2.5 volts).

The electrical length is the same as the positive alternation of the input gate, or 500 microseconds.

The prt is 700 microseconds (500 + 200) and the prf is l/prt or 1,428 hertz.
5.5 BOOTSTRAP SWEEP CIRCUIT:
- In Bootstrap method, linearization is achieved with positive feedback.
- In Miller voltage sweep generator, we have used negative feedback for linearization purpose.
- The principle of the Bootstrap circuit can be understood from the figure.

![Exponential RC circuit](image1)

**Fig: exponential RC circuit**

![Capacitor voltage and current waveforms in exponential sweep circuit](image2)

**Fig: Capacitor voltage and current waveforms in exponential sweep circuit**

In the simple RC circuit, let the switch s be closed at time $t=0$. Then we have

\[ V_c \big|_{t=0} = 0 \]  
\[ i_c \big|_{t=0} = \frac{V_x}{R} \]  

For the time interval $0 < t < \infty$ we have

\[ V_c = V_x[1 - \exp(-t/RC)] \]  
\[ i_c = [i_c \big|_{t=0}]\exp(-t/RC) \]

- The figure shows the plots of the wave forms of voltage $V_c$ and current $i_c$.
- It may be seen that the current decays exponentially while the voltage rises exponentially towards steady state value $V_s$.
- One of the methods of sweep linearization is charge the capacitor $C$ through a constant current source.
- Alternatively, from equation 4, it may be inferred that as $V_c$ raises, supply voltage, $V_x$ can be made to rise suitably such that the charging current remains constant.
- In Bootstrap method, this is achieved by positive feedback.
Figure below, shows the circuit arrangement of Bootstrap linear voltage sweep generator. The feedback resistor $R$ provides the positive feedback.

![Bootstrap Circuit Diagram](image)

**Fig:** General bootstrap circuit employing positive feedback for sweep linearization.

![Equivalent Circuit Diagram](image)

**Fig:** Equivalent circuit of general bootstrap sweep circuit.

![Capacitor Voltage Graph](image)

**Fig:** Capacitor voltage for different values of amplifier gain.

- The capacitor $C$ is a timing capacitor.
- In the voltage across $C$, at any time after the switch is opened, is denoted $v_c$.
- This voltage is amplified by the amplifier and the output voltage is given by

$$V_0 = Av_0 + v_{dc}$$

- Where $A$ is the amplifier gain and $v_{dc}$ is the dc level of the amplifier at the output terminals.
- The dc level $v_{dc}$ is a necessary requirement due to special nature of the circuit.
- In the absence of such a dc level, the capacitor $C$ will not begin to charge when the switch $S$ is open.
- The charging current
From the eq. 7, we see that to keep the charging current $ic$ constant, the amplifier gain must be positive and have unity magnitude.

The steady state voltage to which the capacitor $C$ can charge may be obtained from the fact that in steady state, charging current $ic$ is 0.

Hence equating $ic = 0$, we get

$$Vc(\infty) = \frac{Vdc}{(1 - A)}$$

At any instant of time the voltage $vc$ across the capacitor $C$ is given by,

$$v0(t) = \frac{1}{C} \int ic dt$$

on differentiating eq 10 with respect to time $t$ we get,

$$\frac{dv0}{dt} + \frac{1 - A}{CR} = \frac{1}{CR} vdc$$

For linear sweep generation we substitute unity for amplifier gain $A$ in eq 12 to get

$$Ic,lin = \frac{Vdc}{R}$$

Charging current given by eq 13 implies that in the equivalent circuit of figure the conductance $G0$ has zero magnitude.

The voltage across the capacitor $C$ is given by

$$Vc,lin = \frac{vdc}{t}$$
5.6 MILLER TOOTH GENERATOR:

- Figure below gives the circuit of a BJT Miller Voltage Sweep Generator.
- By using negative current feedback the current flowing in the timing capacitor C is kept constant.
- To understand the operation assume the switch s to be ideal.

![Miller sawtooth generator diagram](image)

- Normally the switch s remains closed and transistor T1 is off.
- The timing capacitor C is charged to a voltage Vcc through the resistor Rc and switch S.
- At time t = 0, switch a opens and the base emitter voltage of transistor T1 increases to Vbe, on.
- This increase in the base emitter voltage is coupled via the capacitor C to the output and there results step rise in the output voltage at t-0 as shown in the figure.

![Output voltage wave in Miller sawtooth generator](image)

- But the conduction through transistor T1, causes a decrease in the voltage Vce of the transistor.
- This decrease in Vce is coupled to the base terminal via the capacitor C thereby preventing the emitter base junction of the transistor T1 from being heavily biased.
- This current i1 and voltage vbe remains fairly constant.
- If we further assume that i1/=ib, capacitor current if will also be a constant.
- Thus for time t> 0+, capacitor C discharges linearly and the output voltage also decrease linearly.
SWEEP TIME PERIOD:

Applying Kirchhoff’s current law at the base node we get equations

\[
\frac{V_{cc} - V_{be}}{R_b} = i_b + i_F
\]

1

Similarly applying KCL at the collector node, we get

\[
\frac{V_{cc} - V_0}{R_c} + i_F = i_c + \frac{V_0}{R_L}
\]

2

The current through the timing capacitor is given by

\[
i_F = \frac{C \cdot d(V_{be} - V_0)}{dt}
\]

3

➤ We assume that \( V_{be} \) remains constant.
➤ The output voltage at \( t=0 \) is given by

\[
V_0(0^-) = \frac{V_{cc} \cdot R_L}{R_c + R_L}
\]

4

Combining eq 1, 2 and 3 we get

\[
V_0(t) = \left[ \frac{RL}{RL + RC} \right] \left[ (A + V_{cc}e^{-t/\tau_{eff}} - A) \right]
\]

5

\[
A = V_{cc} \left[ \frac{\beta R_c}{R_b} - 1 \right] - \frac{\beta V_{be} R_c}{R_b}
\]

6

\[
\tau_{eff} = C \frac{R_c R_L}{R_c + R_L} (\beta + 1)
\]

7

➤ It may be seen from eq 7 that the effective time constant gets multiplied by the factor \( \beta + 1 \) due to feedback.
➤ On assuming that \( T_s < \tau_{eff} \) the output voltage decreases linearly with time as shown in the figure.

On substituting \( \alpha F = \beta / (\beta + 1) \) in eq 5 we get

\[
V_0(t) = \frac{V_{cc} \cdot R_L}{R_c + R_L} - \frac{V_{cc} - V_{be}}{CR_b} \cdot t \cdot \alpha F
\]

8

At \( t = T_s \), \( V_s = V_{ce} \) (sat)
Thus the transistor is saturated and the ramp terminates.

The output voltage becomes a constant at \( V_{ce} \text{ (sat)} \).

If we substitute \( t = \infty \) in equation 7 we get

\[
v_0(\infty) = -\frac{A RL}{R_c + RL} \approx -\frac{\beta V_{cc} R_c}{R_b}
\]

Thus the steady voltage to which the transistor can charge theoretically is also increased.

RECOVERY:

When the switch is again closed the output voltage rises with the time constant \( C[R_c.R_L/(R_c+R_L)] \) towards \( V_{cc} \).

Thus retrace time interval may be negligible.

Retrace period can be taken as 4 to 5 times the retrace time constant.

To enhance linearity of the above circuit, it is necessary that the transistor should have very high value of forward current gain.

An alternative approach is to use the transistor in Darlington configuration.

5.7 CURRENT TIME BASE GENERATOR:

A current time base generator provides a current waveform, which increases linearly with time.

Such current time base generators are used in television deflection systems, where magnetic deflection is employed for greater deflection sensitivity.

It also finds wide application in radar.

A simple current time base generator circuit and gating waveform is shown below:

![Current Sweep Circuit](image)

**Fig(a) : A current sweep circuit**

The transistor is initially in the OFF state.

At time \( t=0 \), current \( i_2 \) through the coil of inductance \( L \) is zero.

When an input gating pulse of width \( t_p \), with a voltage \( V_{vi} \) is applied, current \( i_L \) increases linearly with time \( t \) during the pulse interval of \( t \) the linear variation of \( L \) is given by,
\[ i_L = \frac{V_{CC}}{L} \]

- During this sweep interval, diode D does not conduct since it is reverse biased.
- The sweep terminates at \( t = t_p \), when the gating signal drives the transistor to cut off.
- Then \( i_L \) continues to flow through D and RD until it decays exponentially to zero.
- During the discharge period, the current through the inductor, \( i_L \), decreases exponentially as given by,
  \[ i_L = I_L e^{-\frac{R}{D}(t-t_p)} \]

- Where \( I_L \) is the maximum value of current flowing through the inductor L.
- For improved linearity of the current sweep, coil resistance must be kept small.

Fig(b) gating waveform (c) the inductor current waveform (d) the waveform of the collector voltage.

**LINEARITY CORRECTION IN CURRENT SWEEP GENERATOR:**

To improve the linearity of current sweep generator, there exist a variety of methods:
- Adjustment of driving waveform
- Linearization by current Boot-strap technique
- Linearity compensating coil.